REMARKS

Claims 1-56 and 82-98 are pending, of which claims 38-56 have been allowed. Claims 9, 21, and 34 have been amended. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claims 9-10, 21-22, and 34-35 stand objected to as being dependent upon a rejected base claim, but the Office Action states that claims 9-10, 21-22, and 34-35 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims (Office Action, page 7). Accordingly, claims 9, 21, and 34 have been rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 10, 22 and 35 are dependent on, and thus incorporate all the limitations of, amended claims 9, 21 and 34, respectively. Thus, Applicant submits that claims 9-10, 21-22, and 34-35 are allowable.

Claims 1-7, 16-19, 82 and 86-90 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Makihara et al, U.S. Patent No. 5,243,573 (hereinafter "Makihara"). The rejection is respectfully traversed.

Claim 1 recites a circuit for reducing clock signal skew. The circuit comprises "at least a first and second complementary clock signal input/output line" and "first and second inverters." The first and second complementary clock signal input/output line "is connected to receive first and second complementary clock input signals and to transmit first and second complementary clock output signals." According to claim 1, "the complementary clock input signals vary between low and high states at regular intervals and have a skewed time lag relative to each other." The first and second inverters "function to reduce the skew present in the complementary clock input signals." Applicant respectfully submits that Makihara fails to disclose the claimed invention.

For example, Makihara, which discloses a sense amplifier circuit is not connected to receive or transmit complementary clock signals. That is, Makihara does not contain any line or circuitry connected to receive "complementary clock input signals [that] vary between low and high states at regular intervals" as recited in claim 1. As such, Makihara does not and cannot reduce a timing skew between the clock signals as is also recited in claim 1. Instead, Makihara senses the difference between a data signal and a reference data signal and outputs the recognized signal and its complement on two output lines. No skew adjustment is conducted in the disclosed circuit. The portions cited in the Office Action (Fig. 2, etc.) disclose that the outputs N4 and N5 are being utilized to output a data signal and its complement (col. 2, lines 36-52; col. 3, lines 14-41); no input or output of complementary clock signals is disclosed. As such, the claimed invention is patentable over Makihara.

The Office Action, however, states that the "voltage at node N4 [in Makihara] is seen to be swung between high voltage level (+V) and ground. Therefore, the signal provided at node N4 meets the definition of 'clock signal' as disclosed in the specification." Office Action at 6. Applicant respectfully traverses this argument.

Because the Makihara circuit is a sense amplifier circuit, the signal at node N4 is a data signal that has been sensed from a bit line. Bit lines do not carry clock signals. Furthermore, the Makihara bit lines do not carry "complementary clock input signals [that] vary between low and high states at regular intervals" (emphasis added) as recited in claim 1 and as set forth in the present specification. As mentioned in the Office Action, the signals seen at node N4 are controlled by a /BE signal. The signal /BE is explicitly disclosed as a data signal (see FIG. 3). Since the /BE signal is generated only when the Makihara application requires the sensing of data, there are no "regular intervals" in which signals are applied to node N4. Moreover, there are no "regular intervals" in which the data signal /BE causes node N4 to have signals that switch from high to low.

In addition, because the information being sensed at node N4 is data read from memory, there is no guarantee that the data will even transition between high and low states as a clock signal must do each and every cycle. Thus, there is no way that the signals at node N4 could be reasonably interpreted as clock signals. Accordingly, claim 1 is patentable over Makihara.

The Office Action further states that "'[s]kew adjustment' is seen as inherent because Makihara discloses each and every components as well as their interconnections as required by claim 1." Office Action at 6. Applicant respectfully disagrees. As set forth above, Makihara does not contain a first and second complementary clock signal input/output line "connected to receive first and second complementary clock input signals and to transmit first and second complementary clock output signals, wherein the complementary clock input signals vary between low and high states at regular intervals and have a skewed time lag relative to each other." As also set forth above, Makihara, which is directed to sense amplifier circuitry for a memory device, discloses the sensing of data signals only. Thus, Makihara only has circuitry connected to receive data, not clock signals. As such, all of the structure of claim 1 is not included in Makihara and thus, clock skew adjustment in Makihara cannot be considered inherent by the Office Action. See M.P.E.P. § 2112.

Claims 2-7 depend from claim 1 and are allowable along with claim 1 for at least the reasons set forth above. Claim 16 recites "at least a first and second complementary clock signal input/output line connected to receive first and second complementary clock input signals and to transmit first and second internal complementary clock signals, wherein the at least first and second complementary clock signals vary between low and high states at regular intervals and have a time lag skew relative to each other" and that "transistors operate to output the at least first and second complementary clock signals with a reduced skew." As set forth above, Makihara fails to disclose these claim elements. As such, claim 16 is patentable over

Makihara for at least the reasons set forth above and on its own merits. Claims 17-19 depend from claim 16 and are allowable along with claim 16.

Claim 82 recites a "method of generating an internal clock signal in an integrated circuit." The method comprises "receiving first and second external clock signals, wherein the first and second external clock signals vary between low and high states at regular intervals, the second external clock signal is an inverse of the first external clock signal and where there exists a time lag skew of one of said external clock signals relative to the other; and modifying the transition of one of said external clock signals relative to the other to produce, from said external clock signals, internal clock signals which have reduced skew."

As set forth above, Makihara, which discloses only sense amplification and sensing of data, fails to disclose these method steps. As such, claim 82 is allowable over Makihara. Claims 86-90 depend from claim 82 and are allowable along with claim 82 for at least the reasons set forth above and on their own merits.

The rejection should be withdrawn and claims 1-7, 16-19, 82 and 86-90 allowed.

Claims 8, 11-13, 20, 23-33, 36-37, 83-85 and 91-98 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Makihara in view of Garcia, U.S. Patent No. 5,949,259. The rejection is respectfully traversed.

Claims 8 and 11-13 depend from claim 1. As such, these claims recite "at least a first and second complementary clock signal input/output line connected to receive first and second complementary clock input signals and to transmit first and second complementary clock output signals, wherein the complementary clock input signals vary between low and high states at regular intervals and have a skewed time lag relative to each other; and first and second inverters each having an input and an

output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second clock signal input/output line, wherein the first and second inverters function to reduce the skew present in the complementary clock input signals."

As set forth above, Makihara fails to disclose these claim limitations. Applicant respectfully submits that Garcia, which has been cited solely as teaching first and second buffer and driver circuits, also fails to disclose, teach or suggest these claim limitations. As such, the combination of Makihara and Garcia fails to teach or suggest all of the limitations of claim 1. Therefore, claims 8 and 11-13 are allowable over the cited combination.

Claims 20 and 23-25 depend from claim 16 and are allowable along with claim 16 for at least the reasons set forth above and on their own merits. Similarly, claims 83-85 depend from claim 82 and are allowable along with claim 82 for at least the reasons set forth above and on their own merits.

Claims 26-33 and 36-37 each recite "at least a first and second complementary clock signal input/output line connected to receive first and second complementary clock input signals and to transmit first and second complementary clock output signals, wherein the complementary clock input signals vary between low and high states at regular intervals and have a skewed time lag relative to each other; and first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second, complementary clock signal input/output line wherein the first and second inverters operate to reduce the skew present in the complementary clock input signals; and a first and second driver circuit, said first and second driver

circuit connected to said first and second clock signal input/output lines, respectively."
As set forth above, the combination of Makihara and Garcia fails to teach or suggest
these limitations. As such, claims 26-33 and 36-37 are allowable over the cited
combincation.

Claims 91-98 each recite a method of generating an internal clock signal in an
integrated circuit. The method of comprises "receiving first and second external clock
signals, wherein the first and second external clock signals vary between low and high
states at regular intervals, the second external clock signal is an inverse of the first
external clock signal and where there exists a time lag skew of one of said external clock
signals relative to the other; buffering each of the first and second external clock signals
using a reference voltage; and modifying the transition of one of said buffered external
clock signals relative to the other to produce, from said buffered external clock signals,
internal clock signals which have reduced skew." As set forth above, Makihara, which
discloses only sense amplification and sensing of data, and Garcia, which arguably
discloses buffer and driver circuits, fail to disclose these method steps. As such, claim
91-98 are allowable over Makihara.

For at least the foregoing reasons, claims 8, 11-13, 20, 23-33, 36-37, 83-85 and
91-98 are allowable over the cited combination. Applicant respectfully submits that the
rejection be withdrawn and the claims allowed.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: March 22, 2004   Respectfully submitted,

By _____

Thomas J. D'Amico
    Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN &
    OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant